GSM 900/DCS 1800 Fractional-N Modulator with Two-Point-Modulation

B. Neurauter [1], G. Märzinger [3], A. Schwarz [3], R. Vuketich [1]
M. Scholz [2], R. Weigel [1,3], J. Fenk [2]
[1]Institute for Communications and Information Engineering, University of Linz, Austria
[2]Infineon Technologies, Munich, Germany
[3]DICE Danube Integrated Circuit Engineering, Linz, Austria

Abstract - **This paper presents a fractional-N modulator architecture that uses the technique of two-point-modulation. This technique allows direct modulation of the VCO within the closed loop of a high resolution PLL based fractional-N frequency synthesizer, without restriction due to loop bandwidth and PLL dynamics.**
A prototype transmitter was implemented using the GSM standard to verify the superior performance predicted by simulation. The core element of this new modulator architecture is a PLL-based fractional-N frequency synthesizer. This prototype synthesizer consists essentially of a full custom IC for the analog section, and the digital functionality was implemented in a filed programmable gate array (FPGA). The analog circuitry was fabricated in a 25 GHz BiCMOS process with 0.8 μm as minimum feature size.
Measurements of the spectrum for the GSM modulated signal and of the demodulated signal show that the strict demands of the GSM specification can be met.

I. Introduction

For modern wireless digital communication systems a variety of modulation schemes are available to achieve an efficient use of the available spectrum. Particulary in handsets the use of low power consumption of nonlinear amplifiers is very attractive. Constant-envelope modulation schemes offer the advantage that nonlinear power amplifiers which have a higher power efficiency than their linear counterparts can be used. Especially in Europe this has led to the introduction of Gaussian filtered Minimum Shift Keying (GMSK) in many wireless systems to limit the spectral bandwidth. Conventional GSM transmitters use quadrature amplitude modulation with separate inphase and quadrature (I/Q) signals that are mixed with a local oscillator. These architecture requires mixers, filter and D/A-converters to translate the inphase and quadrature components of the baseband signals to the desired RF carrier frequency and is typically realized in a heterodyne or homodyne approach.
To achieve a high degree of digital functionality and therefore the possibility of high integration and low power consumption a modulator topology can be developed with a minimum number of building blocks - a Gaussian filter and a PLL-based fractional-N frequency synthesizer [1]. In [2] and [3] methods are presented where the data rate exceeds the closed loop bandwidth of the synthesizer. This is possible due to the use of a digital compensation filter which has the inverse of the closed loop transfer function. But since the loop transfer function is very sensitive to process and temperature variation simulation results in [4] show the problem of mismatch between the digital compensation filter and the analog parameters of the frequency synthesizer.

II. GMSK Modulator Architecture

The proposed modulator architecture aiming to the GSM standard depicted in Fig. 1 uses the technique of two-point-modulation. This technique allows direct modulation of the VCO within the closed loop, without restriction due to loop bandwidth and PLL dynamics

0-7803-7239-5/02/$10.00 © 2002 IEEE

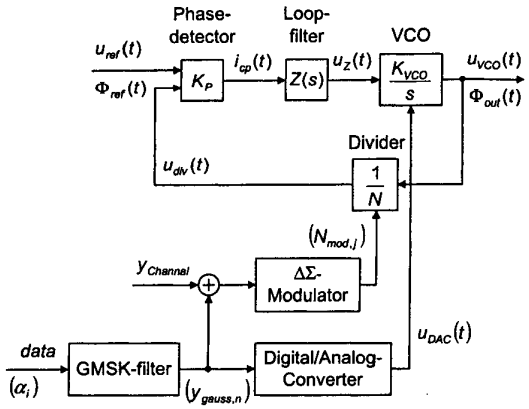

Figure 1: Fractional-N modulator using two-point-modulation

synthesizer as shown in [5] leads to a fundamental characteristic for the transmission of a superimposed signal at the output of a phase locked loop. There are points from which a signal fed into the PLL is filtered by the low-pass transfer function $G(s)$ respectively the high-pass transfer function $1 - G(s)$. The closed-loop transfer function of Fig. 1 can be derived as

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = N\frac{1}{1+\frac{N}{K_P K_{VCO}}\frac{s}{Z(s)}} = NG(s) \quad (1)$$

where N is the divider value, K_P [A/rad] and K_{VCO} [rad/Vs] are the conversion gain values of the PFD and the VCO respectively; $Z(s)$ [Ω] is the Laplace transform of the transimpedance of the loop filter and s is the complex Laplace variable.

III. Modeling

Core element of this new modulator architecture is the in [5] presented Fractional-N Frequency Synthesizer for GSM 900 and DCS 1800. Due to the use of this proposed synthesizer it is possible to induct the modulation signal at the low-pass point directly by the digital ΔΣ-modulator.

With the use of m-bit wide accumulators the digital sequence $(y_{gauss,n})$ is converted by the factor

$$\Delta f_{out,TP} = \frac{f_{ref}}{2^m} \quad (2)$$

and the voltage $u_{DAC}(t)$ by the factor

$$\Delta f_{out,HP} = U_{LSB} S_{VCO} \quad (3)$$

into frequency. In equation (3) $S_{VCO}\left[\frac{\text{MHz}}{\text{V}}\right]$ is the conversion gain value of the VCO and U_{LSB} [V] the voltage level for the least significant bit of the D/A-Converter.

In the complex variable domain the frequency of the VCO $F_{out}(s)$ is given by:

$$\begin{aligned} F_{out}(s) &= [1-G(s)]\,Y_{gauss}(s)\Delta f_{out,HP} \\ &\quad + Y_{gauss}(s)\Delta f_{out,TP}G(s) \\ &\quad + Y_{Channel}\Delta f_{out,TP}G(s) \end{aligned} \quad (4)$$

If $\Delta f_{out,HP}$ is scaled by the formal expression

$$\Delta f_{out,HP} = \Delta f_{out,TP} = U_{LSB} S_{VCO} \quad (5)$$

the transfer function for the modulation signal $Y_{gauss}(s)$ is given by:

$$G(s) + 1 - G(s) = 1. \quad (6)$$

Equation (6) describes mathematically the fact that with the use of the digital sequence $(y_{gauss,n})$ the carrier signal at frequency $f_{Channel}$ - according to $y_{Channel}$ - can be modulated without restriction due to loop bandwidth and PLL dynamics. Fig. 2, 3 and 4 show simulation results for the step responses for the frequency of the output signal $u_{out}(t)$ relative to the channel-frequency of $f_{Channel} = 900\,\text{MHz}$.

Corresponding simulations predict an ideal step re-

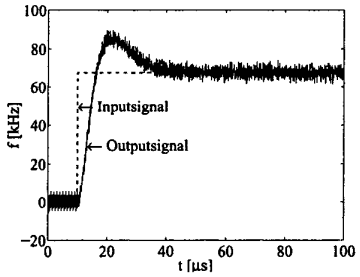

Figure 2: Low-pass step response at channel-frequency $f_{Channel} = 900\,\text{MHz}$

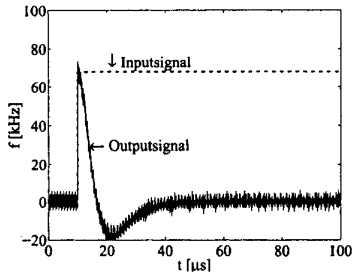

Figure 3: High-pass step response at channel-frequency $f_{Channel} = 900\,\text{MHz}$

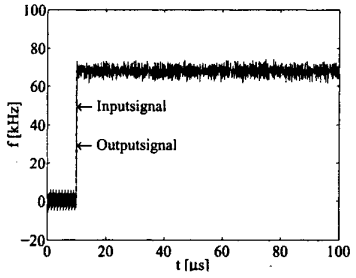

Figure 4: Step response for two-point-modulation at channel-frequency $f_{Channel} = 900\,\text{MHz}$

sponse, as shown in Fig. 4, for a step in frequency up to 80 MHz.

IV. Circuit Realization and Measurement Results

To demonstrate the performance of this modulator architecture a modular test transmitter was built to verify the superior performance predicted by simulation. The fractional-N frequency synthesizer consists essentially of a full custom IC for the analog section and this part is fabricated in a 25 GHz BiCMOS process with 0.8 μm as minimum feature containing a conventional sequential structure as phase-frequency detector (PFD) [6], tri-state charge pump and a new architecture for a multi-modulus divider. The digital MASH $\Delta\Sigma$-modulator is implemented in a field programmable gate array (FPGA) and achieves its speed due to pipelining. Due to the fact that the realized fractional-N frequency synthesizer offers a minimum step size of 12.4 Hz the adjustment of the channel-frequency can be done in a digital manner to perform the required accuracy of 0.1 ppm for the transmitted carrier frequency in GSM. Also a very fast settling time for an applied 75 MHz jump from 1710 MHz to 1785 MHz of smaller than 90 μs is achieved. Furthermore an inband phase noise of up to $-95.5\frac{\text{dBc}}{\text{Hz}}$ in the fractional-mode was measured at 30 kHz offset [7].

The induction of the modulation signal at the low-pass point is directly done by the digital MASH $\Delta\Sigma$-modulator who generates a divider sequence corresponding to the modulation data. To inject the modulation data to the input of the VCO, a new loop-filter topology has been investigated.

Fig. 5 shows measured I and Q eye diagrams from the test transmitter using a vector signal analyzer FSIQ 26. These results with well defined openings and areas of

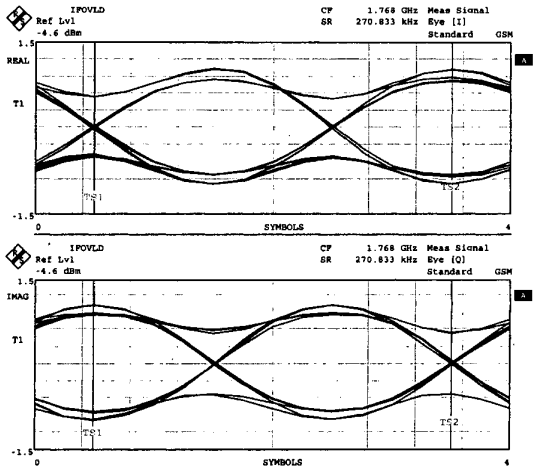

Figure 5: Measured I and Q eye diagrams at $f_{Channel} = 1768\,\text{MHz}$ carrier frequency

compact crossover points indicate the high achievable performance of this modulator architecture based on a fractional-N PLL.

Fig. 6 shows the measured output power spectrum for the GSM modulated RF carrier at $f_{Channel} = 1768\,\text{MHz}$ with random data input, obtained also with an FSIQ 26 spectrum analyzer. The GSM transmit

spectral mask is included to verify that the power spectrum of the modulated carrier is within the specified limits. Further measurements of the spectrum for the

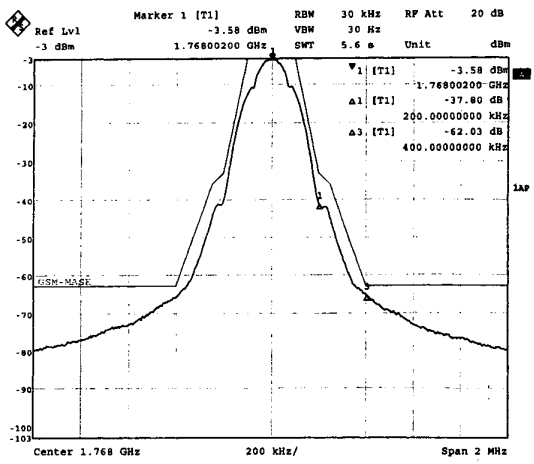

Figure 6: Measured output power spectrum of the fractional-N modulator with two-point-modulation at $f_{Channel} = 1768\,\text{MHz}$ carrier frequency

GSM modulated signal show that with $\phi_{rms} < 1.9°$ and $\phi_{peak} < 5°$ the strict demands of the GSM specification can be met.

V. Conclusion

A new modulator architecture for constant envelope modulation has been described that uses the technique of two-point-modulation. The modulator is based on direct modulation of the VCO within the closed loop of a high resolution PLL based fractional-N frequency synthesizer, without restriction due to loop bandwidth and PLL dynamics. This architecture reduces the complexity and eliminates many of the implementation problems found in conventional GMSK transmitters. A major advantage of this transmitter architecture is the high degree of digital functionality, and therefore is well suited for further monolithic integration in CMOS technology. Using the GSM standard a modular test transmitter was built and measurements show that the requirements of many RF applications especially the strict demands of the GSM specification can be met.

References

[1] B. Miller, J. Conley, "A Multiple Modulator Fractional Divider", *IEEE Transactions on Insturmentation and Measurement*, Vol. 40. No. 3, June 1991, pp. 578-583

[2] M. H. Perrot, T. T. Tewksbury III, C. G. Sodini, "A 27-mW CMOS Fractional-N Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, December 1997, pp. 2048-2060

[3] W. T. Bax, M. A. Copeland, "A GMSK Modulator Using a $\Delta\Sigma$ Frequency Discriminator-Based Synthesizer", *IEEE Journal of Solid-State Circuits*, Vol. 36. No. 8, August 2001, pp. 1218-1227

[4] G. Märzinger, A. Springer, R. Weigel, S. Herzinger, J. Fenk, "FN-Modulation Loop Architecture for Fully Integrated 1 MB/s GFSK Transmitter", *Proceedings of the 1999 IEEE MTT-S International Microwave Symposium*, IEEE MTT-S International Microwave Symposium 99, pp. 1851-1854

[5] B. Neurauter, G. Märzinger, T. Lüftner, R. Weigel, M. Scholz, V. Mutlu, J. Fenk, "Low Phase Noise Frequency-Synthesizer with Very High Frequency-Resolution for GSM 900/DCS 1800", *Proc. European Microwave 2000*, October 2000, pp. 124-127

[6] J. L. Stensby, *Phase-Locked-Loops: Theory and Applications*, CRC Press LLC 1997

[7] B. Neurauter, G. Märzinger, T. Lüftner, R. Weigel, M. Scholz, V. Mutlu, J. Fenk, "GSM 900/DCS 1800 Fractional-N Frequency Synthesizer with Very Fast Settling Time", *IEEE MTT-S International Microwave Symposium 2001*, May 2001, pp. 705-708